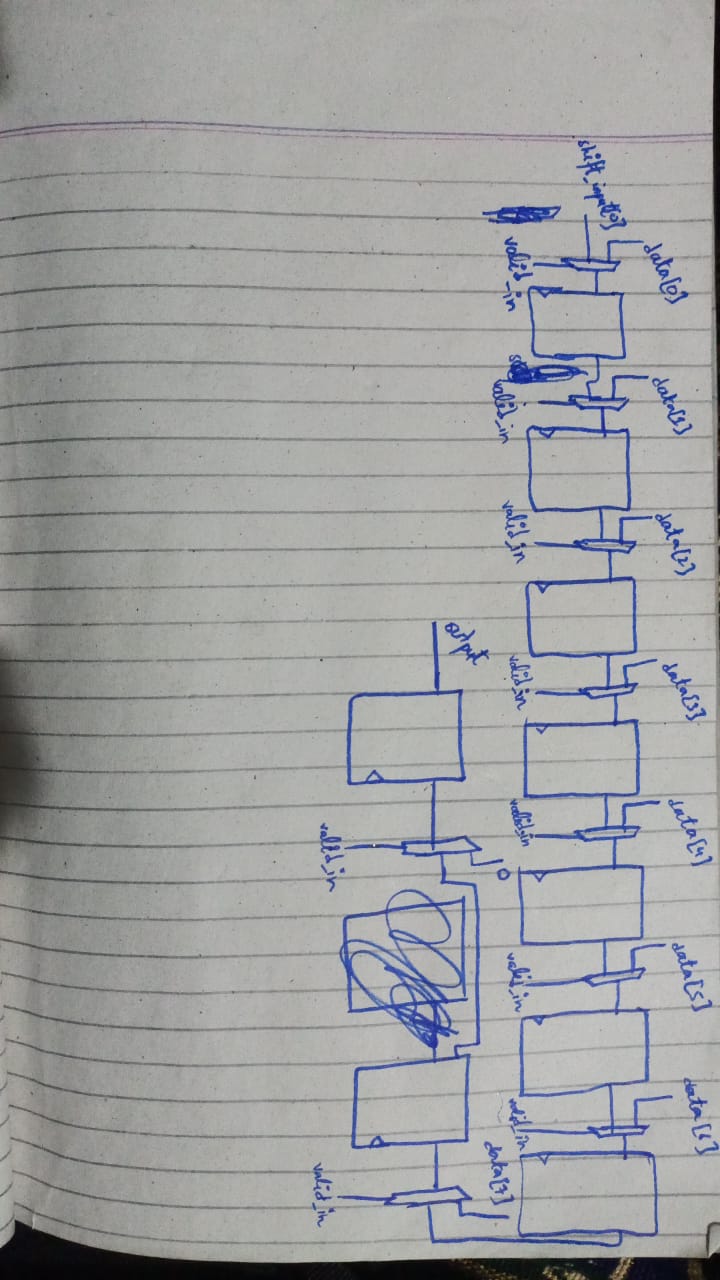
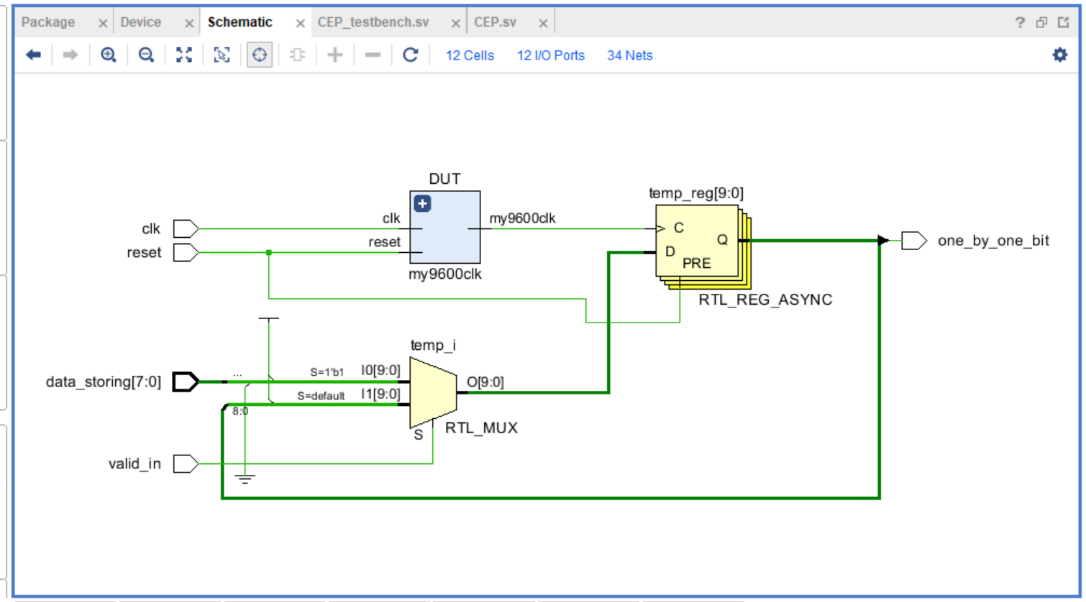
***COMPLEX ENGINEERING PROBLEM***

REPORT

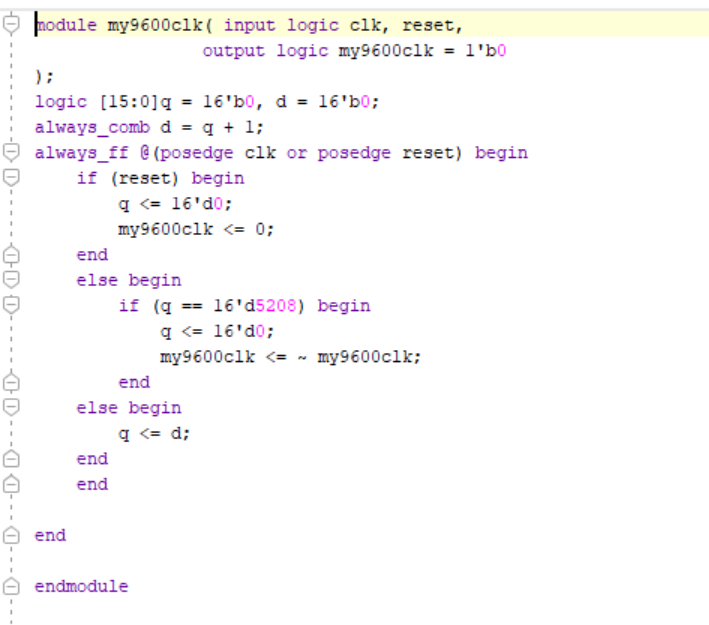
HANDMADE DIAGRAM:



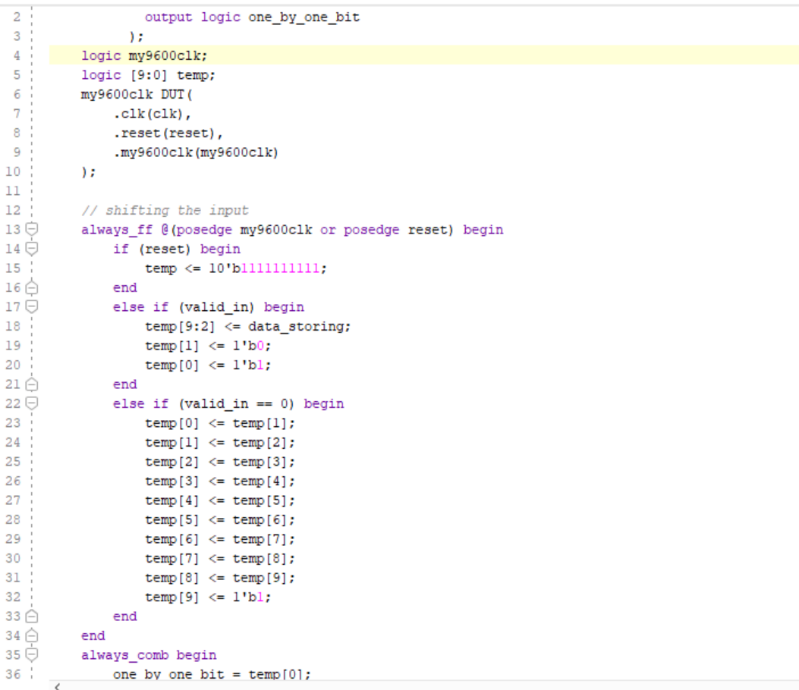
Vivado design:



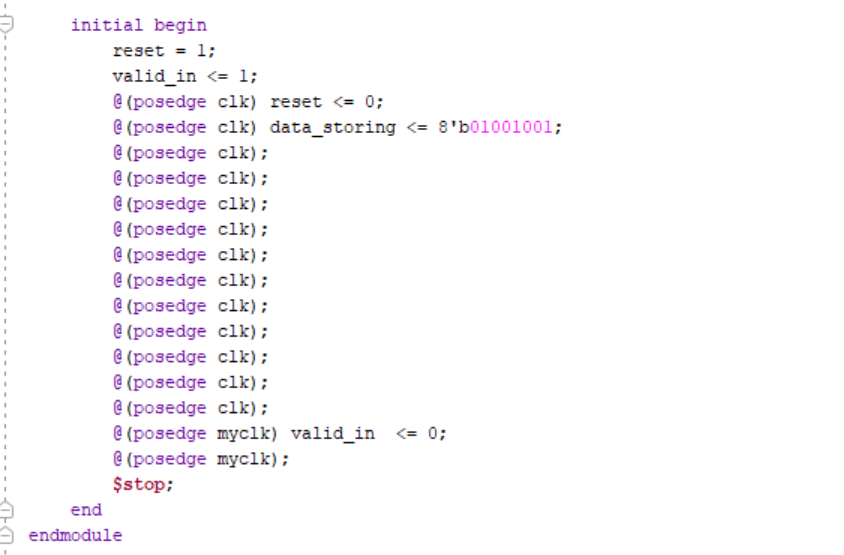
Clock generation:



Code for serial\_out:

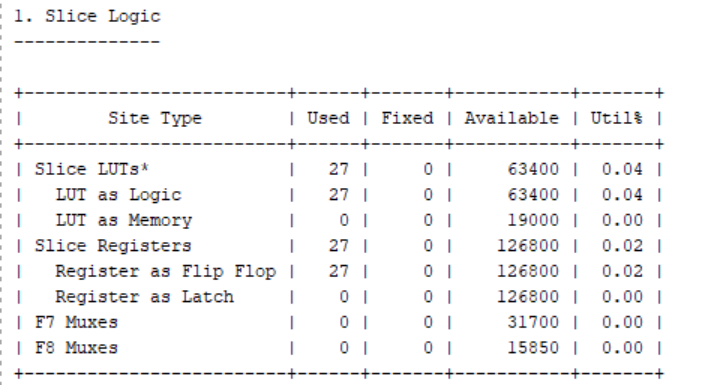


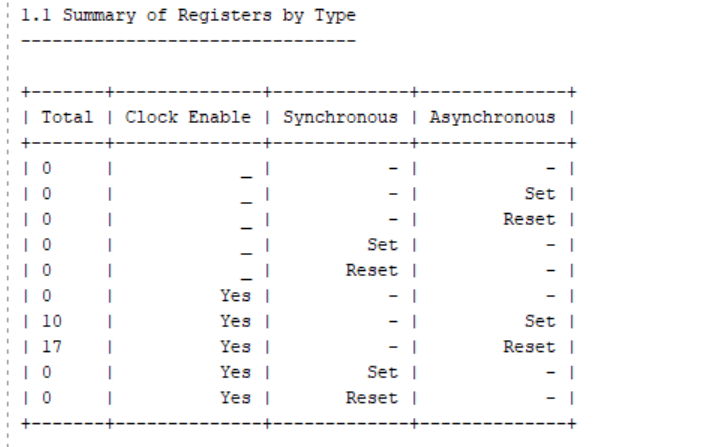
Testbench code:

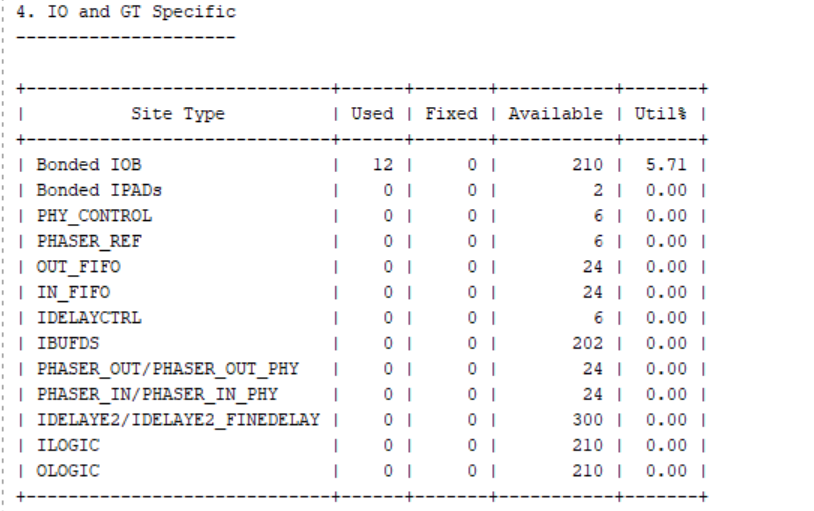


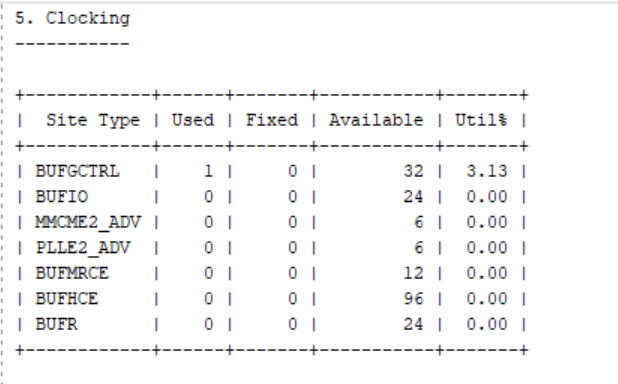
Resource utilization:

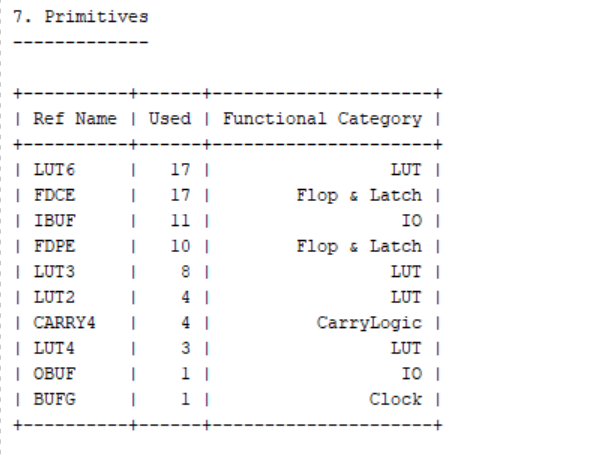
Synthesis:

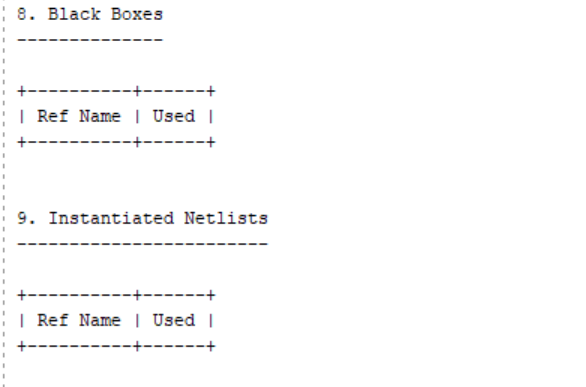




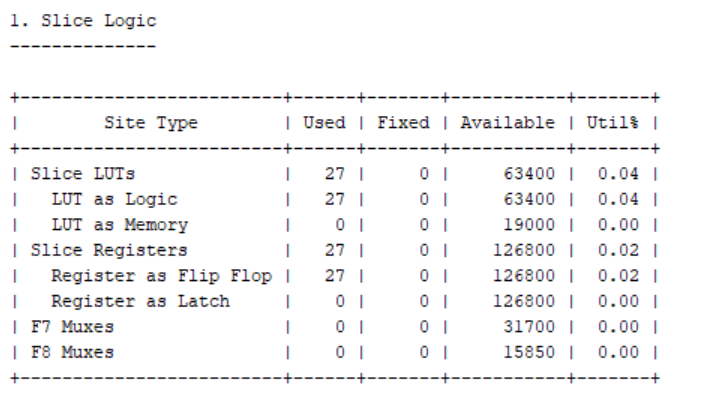


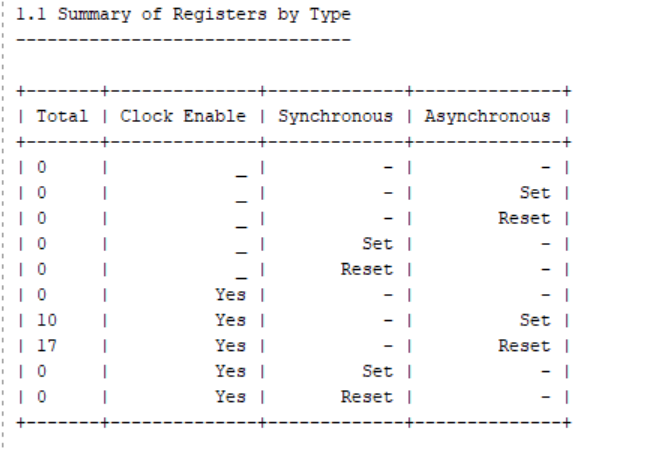


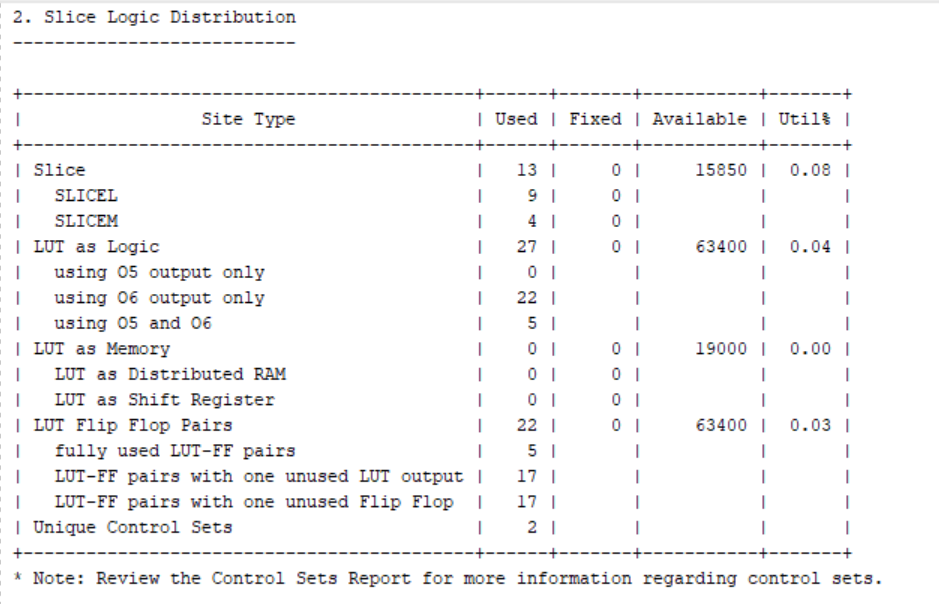


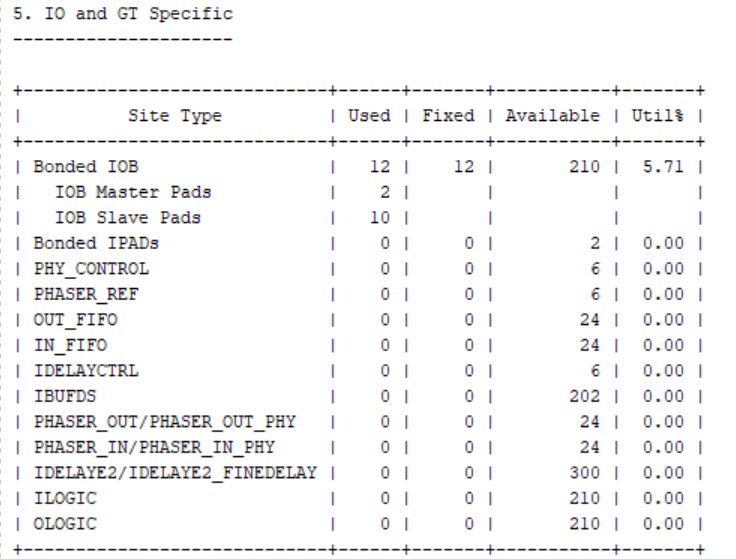


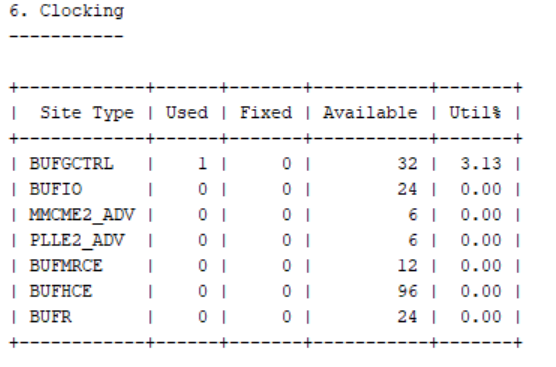
Implementation:

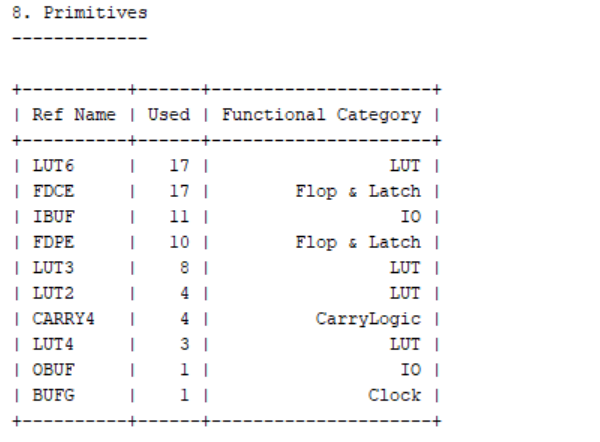


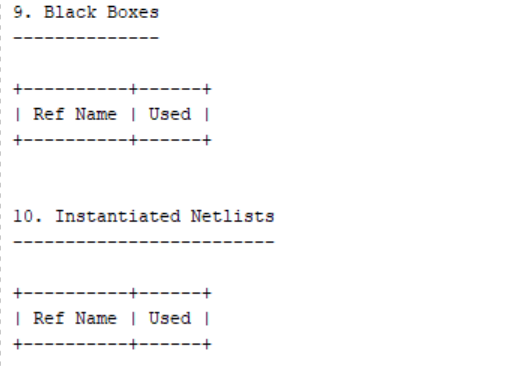






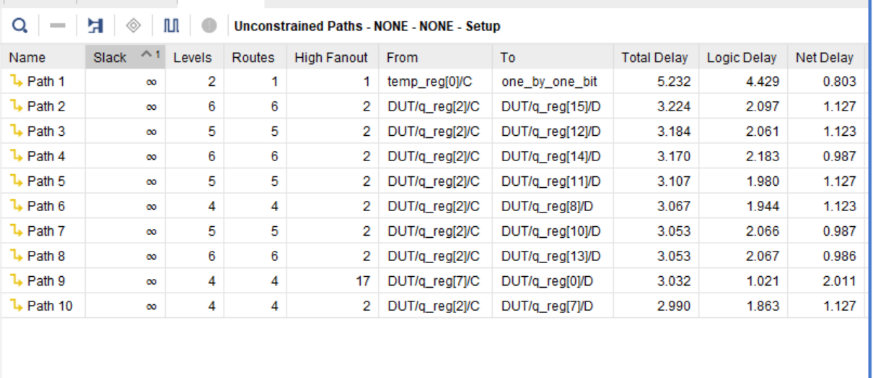


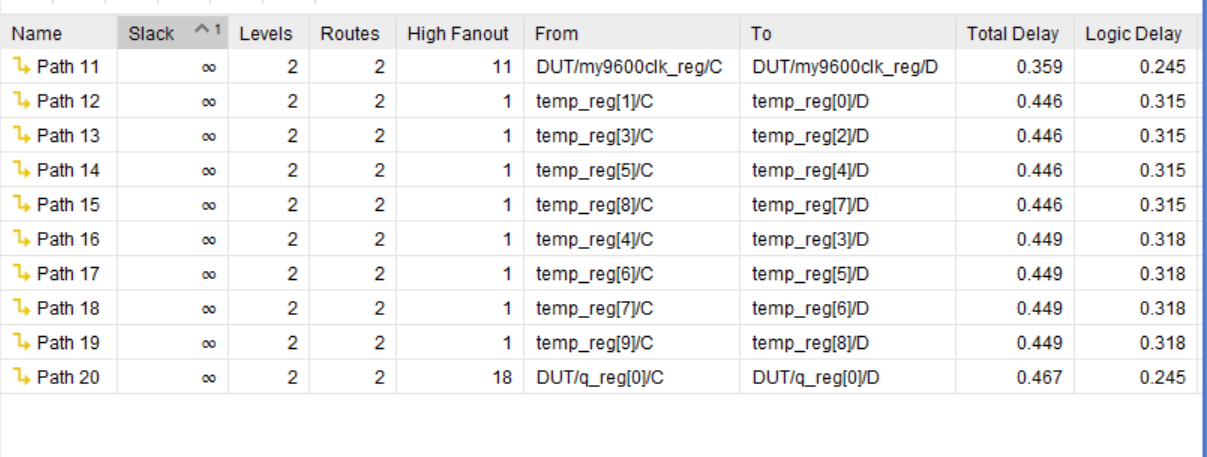




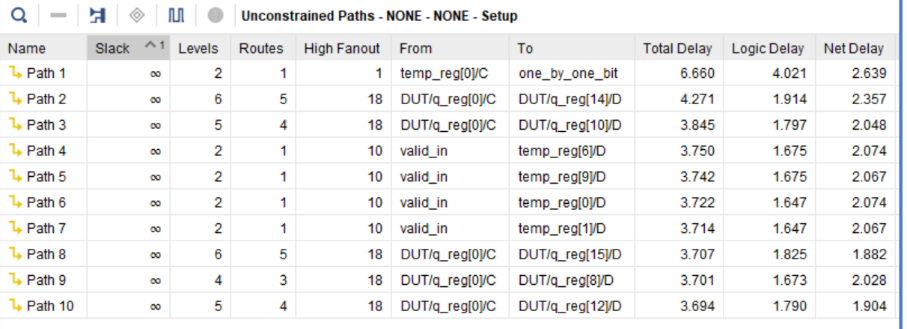
Timing summary:

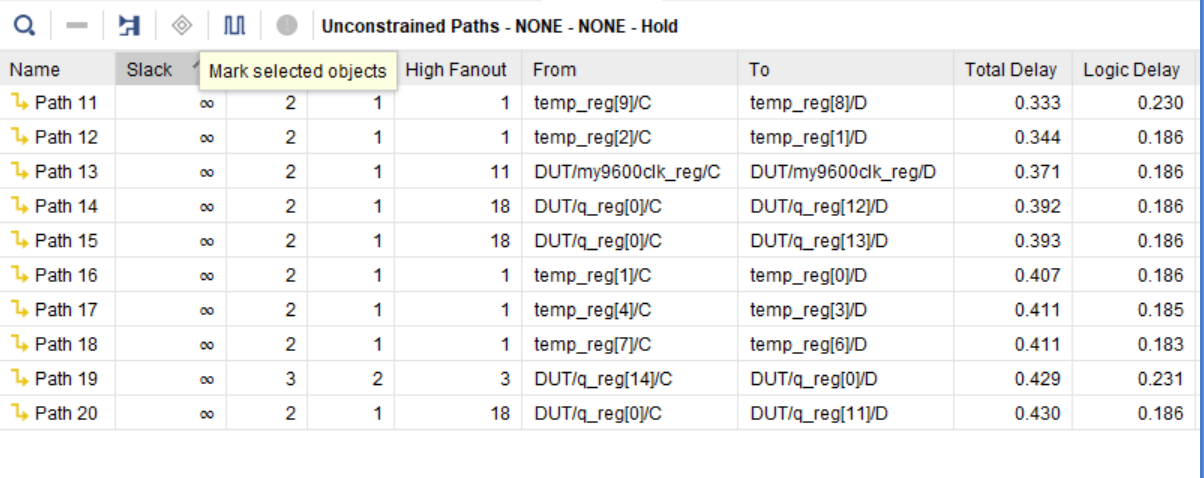
Synthesis:



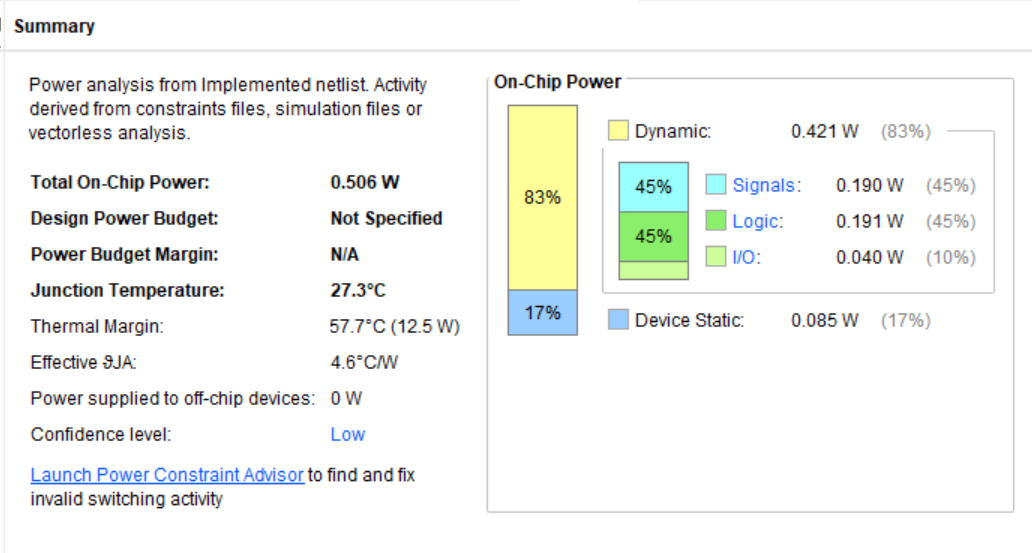


Implementation:





Power generation:



Simulation results:

